1 **PROCESSING ARCHITECTURE**
2 .Vector processor
3 ..Scalar/vector processor interface
4 ..Distributing of vector data to vector registers
5 ...Masking to control an access to data in vector register
6 ..Controlling access to external vector data
7 ..Vector processor operation
8 ...Sequential
9 ...Concurrent
10 .Array processor
11 ..Array processor element interconnection
12 ...Cube or hypercube
13 ...Partitioning
14 ...Processing element memory
15 ...Reconfiguring
16 ..Array processor operation
17 ...Application specific
18 ...Data flow array processor
19 ...Systolic array processor
20 ...Multimode (e.g., MIMD to SIMD, etc.)
21 ...Multiple instruction, Multiple data (MIMD)
22 ...Single instruction, multiple data (SIMD)
23 .Superscalar
24 .Long instruction word
25 .Data driven or demand driven processor
26 ..Detection/pairing based on destination, ID tag, or data
27 ..Particular data driven memory structure
28 .Distributed processing system
29 ..Interface
30 ..Operation
31 ...Master/slave
32 .Microprocessor or multichip or multimodule processor having sequential program control
33 ..Having multiple internal buses
34 ..Including coprocessor
35 ...Digital Signal processor
36 ..Application specific
37 ..Programmable (e.g., EPROM)
38 ..Offchip interface
39 ...Externally controlled internal mode switching via pin
40 ...External sync or interrupt signal
41 ..RISC
42 ..Operation
43 ...Mode switching
200 **ARCHITECTURE BASED INSTRUCTION PROCESSING**
201 .Data flow based system
202 .Stack based computer
203 .Multiprocessor instruction
204 **INSTRUCTION ALIGNMENT**
205 **INSTRUCTION FETCHING**
206 .Of multiple instructions simultaneously
207 .Prefetching
208 **INSTRUCTION DECODING (E.G., BY MICROINSTRUCTION, START ADDRESS GENERATOR, HARDWIRED)**
209 .Decoding instruction to accommodate plural instruction interpretations (e.g., different dialects, languages, emulation, etc.)
210 .Decoding instruction to accommodate variable length instruction or operand
211 .Decoding instruction to generate an address of a microroutine
212 .Decoding by plural parallel decoders
213 .Predecoding of instruction component
214 **INSTRUCTION ISSUING**
215 .Simultaneous issuance of multiple instructions
216 **DYNAMIC INSTRUCTION DEPENDENCY CHECKING, MONITORING OR CONFLICT RESOLUTION**
217 .Scoreboarding, reservation station, or aliasing
218 .Commitment control or register bypass
219 .Reducing an impact of a stall or pipeline bubble
220 **PROCESSING CONTROL**
221 .Arithmetic operation instruction processing
222 ..Floating point or vector
223 .Logic operation instruction processing
224 ..Masking
225 .Processing control for data transfer

226 .Instruction modification based on condition
227 .Specialized instruction processing in support of testing, debugging, emulation
228 .Context preserving (e.g., context swapping, checkpointing, register windowing
229 .Mode switch or change
230 .Generating next microinstruction address
231 .Detecting end or completion of microprogram
232 .Hardwired controller
233 .Branching (e.g., delayed branch, loop control, branch predict, interrupt)
234 ..Conditional branching
235 ...Simultaneous parallel fetching or executing of both branch and fall-through path
236 ...Evaluation of multiple conditions or multiway branching
237 ...Prefetching a branch target (i.e., look ahead)
238 ....Branch target buffer
239 ...Branch prediction
240 ....History table
241 ..Loop execution
242 ..To macro-instruction routine
243 ..To microinstruction subroutine
244 ..Exception processing (e.g., interrupts and traps)
245 .Processing sequence control (i.e., microsequencing)
246 ..Plural microsequencers (e.g., dual microsequencers)
247 ..Multilevel microcontroller (e.g., dual-level control store)
248 ..Writable/changeable control store architecture
300 **BYTE-WORD REARRANGING, BIT-FIELD INSERTION OR EXTRACTION, STRING LENGTH DETECTING, OR SEQUENCE DETECTING**

FOREIGN ART COLLECTIONS

FOR 000 **CLASS-RELATED FOREIGN DOCUMENTS**